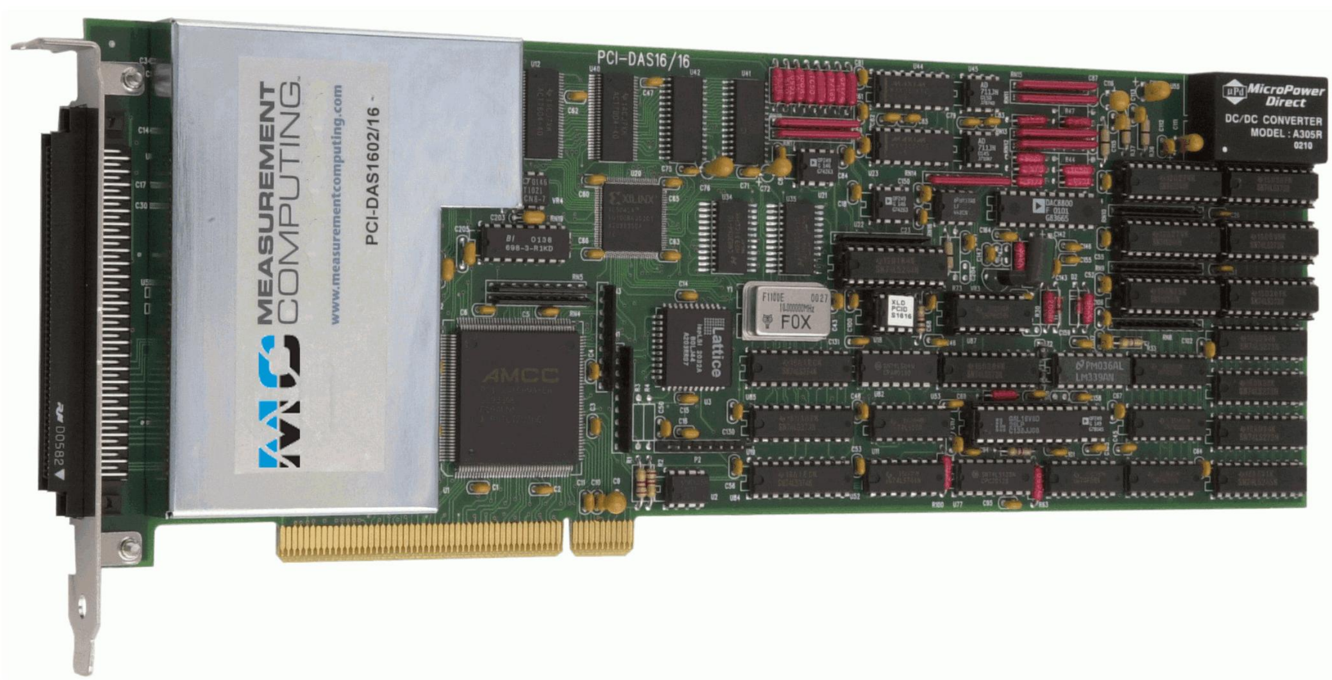
PCI-DAS1602/16

Analog and Digital I/O Board

User's Guide



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Document Revision 7, March, 2009

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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide explains how to install, configure, and use the PCI-DAS1602/16 board so that you get the most out of its analog, digital, and timing I/O features.

This user's guide also refers you to related documents available on our web site, and to technical support resources.

Conventions in this user's guide

For more information on …

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#>	Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.
bold text	**Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example: **1.** Insert the disk or CD and click the **OK** button.
italic text	*Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example: The *Insta*Cal installation procedure is explained in the *Quick Start Guide*. *Never* touch the exposed pins or circuit connections on the board.

Where to find more information

The following electronic documents provide helpful information relevant to the operation of the PCI-DAS1602/16.

- MCC's *Specifications: PCI-DAS1602/16* (the PDF version of the *Specifications* chapter in this guide) is available on our web site at www.mccdaq.com/pdfs/Specs/PCI-DAS1602-16-spec.pdf.
- MCC's *Quick Start Guide* is available on our web site at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.
- MCC's *Guide to Signal Connections* is available on our web site at www.mccdaq.com/signals/signals.pdf.
- MCC's *Universal Library User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf.
- MCC's *Universal Library Function Reference* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-functions.pdf.
- MCC's *Universal Library for LabVIEW™ User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/SM-UL-LabVIEW.pdf.

PCI-DAS1602/16 User's Guide (this document) is also available on our web site at www.mccdaq.com/PDFmanuals/PCI-DAS1602-16.pdf.

Introducing the PCI-DAS1602/16

Overview: PCI-DAS1602/16 features

The PCI-DAS1602/16 multifunction analog and digital I/O board sets a new standard for high performance data acquisition on the PCI bus. This manual explains how to install and use the PCI-DAS1602/16 board.

The PCI-DAS1602/16 is a multifunction measurement and control board designed for the PCI bus. This board can be used for applications such as data acquisition, system timing, and industrial process control.

The PCI-DAS1602/16 board is completely plug and play, with no switches, jumpers or potentiometers to set. All board addresses and interrupt sources are set with software. You calibrate the board with software that uses programmable on-board digital potentiometers and trim D/A converters.

The PCI-DAS1602/16 provides the following features:

- Eight differential or 16 single-ended 16-bit analog inputs
- Sample rates of up to 200 kHz
- 24 bits of high-drive digital I/O
- Three 16-bit down counters
- 100-pin high density I/O connector
- Two FIFO buffered 16-bit analog outputs with update rates of up to 100 kHz

Analog input ranges are selectable via software as bipolar or unipolar. Bipolar input ranges are ±10 V, ±5 V, ±2.5 V and ±1.25 V. Unipolar input ranges are 0 to 10 V, 0 to 5 V, 0 to 2.5 V and 0 to 1.25 V. The PCI-DAS1602/16 has an analog trigger input. The trigger level and direction are software configurable.

The PCI-DAS1602/16 board has two 82C54 counter chips. Each chip contains three 16-bit down counters that provide clock, gate, and output connections.

Software features

For information on the features of *Insta*Cal and the other software included with your PCI-DAS1602/16, refer to the *Quick Start Guide* that shipped with your device. The *Quick Start Guide* is also available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Check www.mccdaq.com/download.htm for the latest software version.

Installing the PCI-DAS1602/16

What comes with your PCI-DAS1602/16 shipment?

The following items are shipped with the PCI-DAS1602/16.

Hardware

- PCI-DAS1602/16

Additional documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). This booklet supplies a brief description of the software you received with your PCI-DAS1602/16 and information regarding installation of that software. Please read this booklet completely before installing any software or hardware.

Optional components

- Cables

C100FF-x

- Signal termination and conditioning accessories

  MCC provides signal conditioning and termination products for use with the PCI-DAS1602/16. Refer to Field wiring and signal termination on page 13 for a complete list of compatible accessory products.

Unpacking the PCI-DAS1602/16

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the PCI-DAS1602/16 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Installing the software

Refer to the *Quick Start Guide* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Installing the PCI-DAS1602/16

The PCI-DAS1602/16 board is completely plug-and-play, with no switches or jumpers to set. Configuration is controlled by your system's BIOS. To install your board, follow the steps below.

Install the MCC DAQ software before you install your board

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

1. Turn your computer off, open it up, and insert your board into an available PCI slot.
2. Close your computer and turn it on.

   If you are using an operating system with support for plug-and-play (such as Windows 2000 or Windows XP), a dialog box opens as the system loads, indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you are prompted for the disk containing this file. The *Measurement Computing Data Acquisition Software* CD supplied with your board contains this file. If required, insert the disk or CD and click **OK**.
3. To test your installation and configure your board, run the *Insta*Cal utility installed in the previous section. Refer to the *Quick Start Guide* that came with your board for information on how to initially set up and load *Insta*Cal.

If your board has been powered-off for more than 10 minutes, allow your computer to warm up for at least 15 minutes before acquiring data with this board. This warm-up period is required for the board to achieve its rated accuracy. The high speed components used on the board generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for more than 10 minutes.

Configuring the PCI-DAS1602/16

All hardware configuration options on the PCI-DAS1602/16 are software controlled. You can select some of the configuration options using *Insta*Cal, such as the analog input configuration (16 single-ended or eight differential channels), the edge used for triggering when using an external pacer, and the counter source. Once selected, any program that uses the Universal Library initializes the hardware according to these selections.

Connecting the board for I/O operations

Connectors, cables – main I/O connector

The table below lists the board connectors, applicable cables, and compatible accessory products for the PCI-DAS1602/16.

Board connector, cables, and accessory equipment

Connector type	100-pin high-density Robinson-Nugent	
Compatible cables	C100FF-x	
Compatible accessory products with the C100FF-x cable	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100	SCB-50 SSR-RACK24 (DADP-5037 adaptor required) SSR-RACK08 (DADP-5037 with TN-MC78M05CT adaptor required) CIO-ERB24 (DADP-5037 adaptor required) CIO-ERB08 (DADP-5037 adaptor required) CIO-SERB08 (DADP-5037 adaptor required)

The PCI-DAS1602/16 board's main I/O connector is a 100-pin high density connector labeled **J1**. All signals pass through this connector. The pinout for eight-channel differential mode is shown on page 11. The pinout for 16-channel single ended mode is shown on page 12.

Information on signal connections

General information regarding signal connection and configuration is available in the *Guide to Signal Connections* (available at www.mccdaq.com/signals/signals.pdf).

Caution! When connecting a cable to the board's I/O connector, make sure that the arrow indicating pin 1 on the board connector lines up with the arrow indicating pin 1 on the cable connector. Connecting cables can damage the board and the I/O controller.

Pinout – main I/O connector

8-channel differential mode pin out

Signal Name	Pin			Pin	Signal Name
GND	100	■	■	50	GND
EXTERNAL INTERRUPT	99	■	■	49	SSH OUT
N/C	98	■	■	48	PC +5 V
EXTERNAL D/A PACER GATE	97	■	■	47	N/C
D/A INTERNAL PACER OUTPUT	96	■	■	46	N/C
A/D INTERNAL PACER OUTPUT	95	■	■	45	A/D EXTERNAL TRIGGER IN
N/C	94	■	■	44	D/A EXTERNAL PACER IN
N/C	93	■	■	43	ANALOG TRIGGER IN
-12 V	92	■	■	42	A/D EXTERNAL PACER
GND	91	■	■	41	CTR 4 OUT
+12 V	90	■	■	40	CTR 4 GATE
GND	89	■	■	39	CTR 4 CLK
N/C	88	■	■	38	D/A OUT 1
N/C	87	■	■	37	D/A GND 1
N/C	86	■	■	36	D/A OUT 0
N/C	85	■	■	35	D/A GND 0
N/C	84	■	■	34	N/C
N/C	83	■	■	33	N/C
N/C	82	■	■	32	N/C
N/C	81	■	■	31	N/C
N/C	80	■	■	30	N/C
N/C	79	■	■	29	N/C
N/C	78	■	■	28	N/C
N/C	77	■	■	27	N/C
N/C	76	■	■	26	N/C
N/C	75	■	■	25	N/C
FIRSTPORTC Bit 7	74	■	■	24	N/C
FIRSTPORTC Bit 6	73	■	■	23	N/C
FIRSTPORTC Bit 5	72	■	■	22	N/C
FIRSTPORTC Bit 4	71	■	■	21	N/C
FIRSTPORTC Bit 3	70	■	■	20	N/C
FIRSTPORTC Bit 2	69	■	■	19	N/C
FIRSTPORTC Bit 1	68	■	■	18	LLGND
FIRSTPORTC Bit 0	67	■	■	17	CH7 LO
FIRSTPORTB Bit 7	66	■	■	16	CH7 HI
FIRSTPORTB Bit 6	65	■	■	15	CH6 LO
FIRSTPORTB Bit 5	64	■	■	14	CH6 HI
FIRSTPORTB Bit 4	63	■	■	13	CH5 LO
FIRSTPORTB Bit 3	62	■	■	12	CH5 HI
FIRSTPORTB Bit 2	61	■	■	11	CH4 LO
FIRSTPORTB Bit 1	60	■	■	10	CH4 HI
FIRSTPORTB Bit 0	59	■	■	9	CH3 LO
FIRSTPORTA Bit 7	58	■	■	8	CH3 HI
FIRSTPORTA Bit 6	57	■	■	7	CH2 LO
FIRSTPORTA Bit 5	56	■	■	6	CH2 HI
FIRSTPORTA Bit 4	55	■	■	5	CH1 LO
FIRSTPORTA Bit 3	54	■	■	4	CH1 HI
FIRSTPORTA Bit 2	53	■	■	3	CH0 LO
FIRSTPORTA Bit 1	52	■	■	2	CH0 HI
FIRSTPORTA Bit 0	51	■	■	1	LLGND

PCI slot ↓

16-channel single-ended mode pin out

Signal Name	Pin		Pin	Signal Name
GND	100	■ ■	50	GND
EXTERNAL INTERRUPT	99	■ ■	49	SSH OUT
N/C	98	■ ■	48	PC +5 V
EXTERNAL D/A PACER GATE	97	■ ■	47	N/C
D/A INTERNAL PACER OUTPUT	96	■ ■	46	N/C
A/D INTERNAL PACER OUTPUT	95	■ ■	45	A/D EXTERNAL TRIGGER IN
N/C	94	■ ■	44	D/A EXTERNAL PACER IN
N/C	93	■ ■	43	ANALOG TRIGGER IN
-12 V	92	■ ■	42	A/D EXTERNAL PACER
GND	91	■ ■	41	CTR 4 OUT
+12 V	90	■ ■	40	CTR 4 GATE
GND	89	■ ■	39	CTR 4 CLK
N/C	88	■ ■	38	D/A OUT 1
N/C	87	■ ■	37	D/A GND 1
N/C	86	■ ■	36	D/A OUT 0
N/C	85	■ ■	35	D/A GND 0
N/C	84	■ ■	34	N/C
N/C	83	■ ■	33	N/C
N/C	82	■ ■	32	N/C
N/C	81	■ ■	31	N/C
N/C	80	■ ■	30	N/C
N/C	79	■ ■	29	N/C
N/C	78	■ ■	28	N/C
N/C	77	■ ■	27	N/C
N/C	76	■ ■	26	N/C
N/C	75	■ ■	25	N/C
FIRSTPORTC Bit 7	74	■ ■	24	N/C
FIRSTPORTC Bit 6	73	■ ■	23	N/C
FIRSTPORTC Bit 5	72	■ ■	22	N/C
FIRSTPORTC Bit 4	71	■ ■	21	N/C
FIRSTPORTC Bit 3	70	■ ■	20	N/C
FIRSTPORTC Bit 2	69	■ ■	19	N/C
FIRSTPORTC Bit 1	68	■ ■	18	LLGND
FIRSTPORTC Bit 0	67	■ ■	17	CH15 HI
FIRSTPORTB Bit 7	66	■ ■	16	CH7 HI
FIRSTPORTB Bit 6	65	■ ■	15	CH14 HI
FIRSTPORTB Bit 5	64	■ ■	14	CH6 HI
FIRSTPORTB Bit 4	63	■ ■	13	CH13 HI
FIRSTPORTB Bit 3	62	■ ■	12	CH5 HI
FIRSTPORTB Bit 2	61	■ ■	11	CH12 HI
FIRSTPORTB Bit 1	60	■ ■	10	CH4 HI
FIRSTPORTB Bit 0	59	■ ■	9	CH11 HI
FIRSTPORTA Bit 7	58	■ ■	8	CH3 HI
FIRSTPORTA Bit 6	57	■ ■	7	CH10 HI
FIRSTPORTA Bit 5	56	■ ■	6	CH2 HI
FIRSTPORTA Bit 4	55	■ ■	5	CH9 HI
FIRSTPORTA Bit 3	54	■ ■	4	CH1 HI
FIRSTPORTA Bit 2	53	■ ■	3	CH8 HI
FIRSTPORTA Bit 1	52	■ ■	2	CH0 HI
FIRSTPORTA Bit 0	51	■ ■	1	LLGND

PCI slot ↓

The signal names for pins 2 to 17 define the functions for both single-ended modes and also for differential input modes. For example, if you are using eight differential inputs, pin 2 is the high side of channel 0 (CH0 HI) and pin 3 is the low side (CH0 LO) of channel 0. If you are using single-ended inputs, pin 2 is channel 0 (CH0 HI), but pin 3 is now channel 8 (CH8 HI). When you use single-ended inputs, use LLGND (and not GND) for analog signal returns.

Cabling

You can use a C100FF-*x* cable to connect signals to the PCI-DAS1602/16 board. The C100FF-x cable is made up of two 50-pin ribbon cables that are joined at one end with a 100-pin connector. The two 50-pin cables diverge and are terminated at the other end with standard 50-pin header connectors.

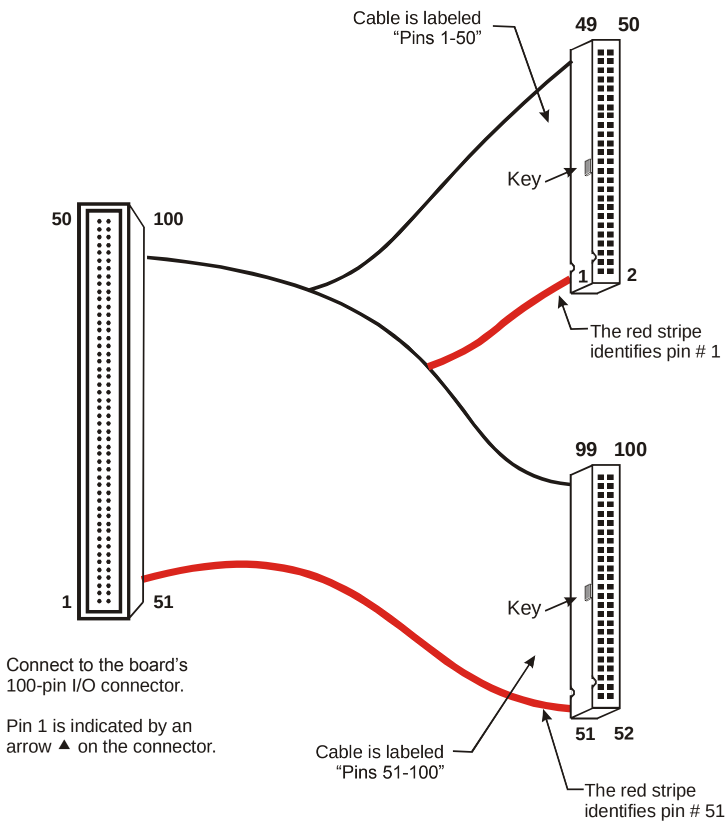

Figure 1. C100FF-*x* cable

The first 50-pin connector is used primarily for analog signals (pins 1-50 on the 100-pin connector). The second 50-pin connector is used primarily for digital signals (pins 51-100 on the 100-pin connector). This configuration minimizes noise in the analog signal lines, and greatly simplifies field wiring and connections to external devices. You can purchase C100FF-x series cables from our web site at www.mccdaq.com/products/accessories.aspx.

Field wiring and signal termination

You can use the following MCC screw terminal boards to terminate field signals and route them into the PCI-DAS1602/16 board using the C100FF-*x* cable:

Screw terminal boards

- **CIO-TERM100** – 100 pin, 16 x 4 screw terminal board.
- **CIO-MINI50** – 50-pin universal screw terminal accessory. Two boards are required.
- **SCB-50** – 50-conductor, shielded signal connection/screw terminal box providing two independent 50-pin connections. One box is required.

Details on these products are available at www.mccdaq.com/products/screw_terminal_bnc.aspx.

BNC connector interface boxes

- **BNC-16SE** – 16-channel single-ended BNC connector box.
- **BNC-16DI** – Eight-channel differential BNC connector box.

Details on these products are available at www.mccdaq.com/products/screw_terminal_bnc.aspx.

Analog signal conditioning and expansion

- **ISO-RACK16/P** – 16-channel isolation module mounting rack.
- **ISO-DA02/P** – Two-channel, 5B module rack.

Details on these products are available at www.mccdaq.com/products/signal_conditioning.aspx.

Digital signal conditioning

The following digital signal conditioning products have 37-pin connectors. Use the DADP-5037 adaptor board for connections to the C100FF-x cable's 50-pin connectors.

- **SSR-RACK24** – 24-position solid state relay rack. The DADP-5037 adaptor board is required.
- **SSR-RACK08** – Eight-channel solid state relay rack. The DADP-5037 with TN-MC78M05CT adaptor board is required.
- **CIO-ERB24** – 24-channel electromechanical relay accessory for digital I/O boards. The DADP-5037 adaptor board is required.
- **CIO-ERB08** – Eight-channel electromechanical relay accessory for digital I/O boards. The DADP-5037 adaptor board is required.

Details on digital signal conditioning products are available at www.mccdaq.com/products/signal_conditioning.aspx. Details on the DADP-5037 adapter board are available at www.mccdaq.com/products/accessories.aspx.

Caution! Before connecting signals to the PCI-DAS1602/16, measure the voltage between ground at the signal source and ground at the PC. If you measure >10 volts, do not connect the board to this signal source, as you are beyond the usable input range of the board. Either adjust your grounding system or add isolation signal conditioning to take useful measurements. A ground offset voltage of more than 30 volts may damage the board and possibly your computer. An offset voltage much greater than 30 volts will damage your electronics, and may be hazardous to your health.

To terminate signals and route them into the PCI-DAS1602/16, use the SCB-50 signal connection box, CIO-TERM100 screw terminal board, or two CIO-MINI50 screw terminal boards.

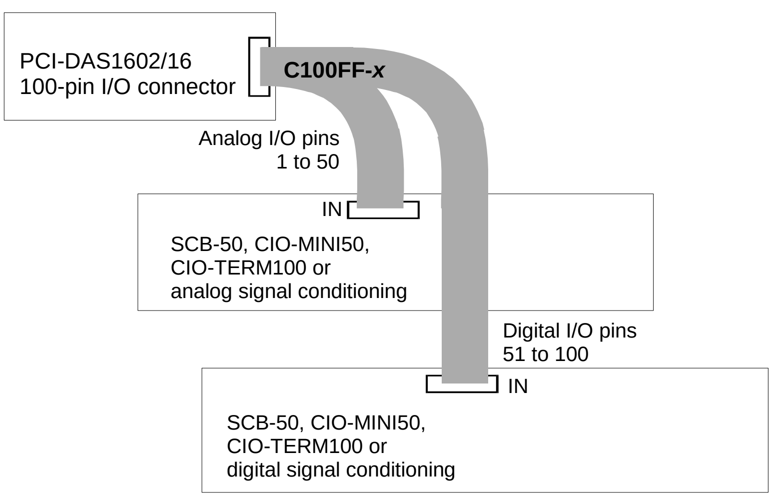

Figure 2. Sample wiring configuration using the C100FF-x cable

Functional Details

PCI-DAS1602/16 block diagram

The PCI-DAS1602/16 provides the following features:

- 16 single-ended or eight fully differential 16-bit analog inputs
- Two 16-bit analog outputs
- 24-bits, high current digital I/O
- Three 16-bit down counters

PCI-DAS1602/16 functions are illustrated in the block diagram shown here.

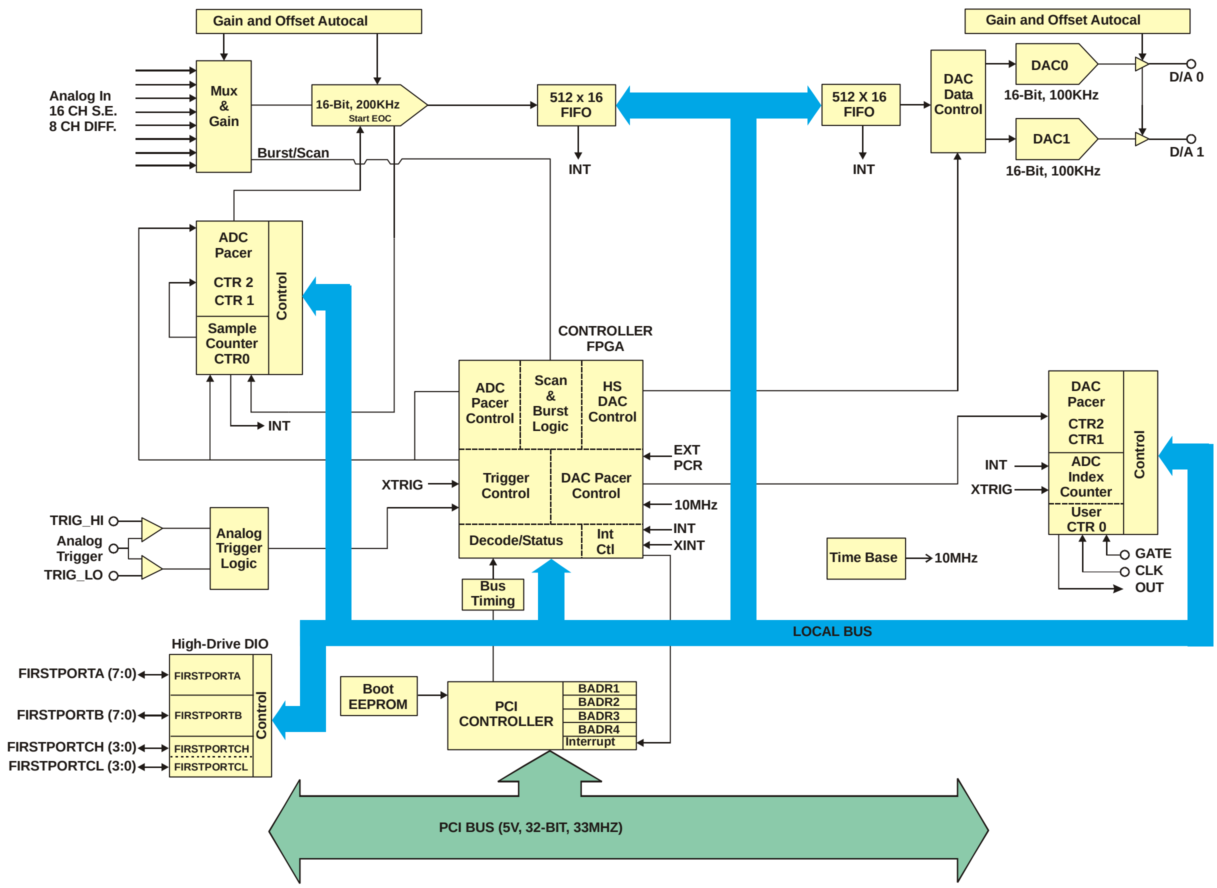

Figure 3. PCI-DAS1602/16 functional block diagram

Analog inputs

The analog input mode is software-selectable for eight differential or 16 single-ended analog inputs. The board offers a 200 kHz maximum sample rate in single and multichannel scans at any gain setting. A 512 sample FIFO assures that data taken from the board is transferred into computer memory without the possibility of missed samples. The board has an analog trigger input with software-selectable trigger levels and direction.

Software selects the bipolar/unipolar input configuration and input range. The table below lists the analog input ranges and resolutions for the available input configurations and gains.

Input range and resolution

Bipolar Range	**Resolution**	**Unipolar Range**	**Resolution**
±10 V	305 µV	0 to 10 V	153 µV
±5 V	153 µV	0 to 5 V	76.3 µV
±2.5 V	76.3 µV	0 to 2.5 V	38.1 µV
±1.25 V	38.1 µV	0 to 1.25 V	19.1 µV

Burst mode

Channel-to-channel skew results from multiplexing the A/D inputs. It is defined as the time between consecutive samples. For example, if four channels are sampled at a rate of 1 kHz per channel, the channel skew is 250 µs (1 ms/4).

Burst mode minimizes channel-to-channel skew by clocking the A/D at the maximum rate between successive channels. Burst mode timing is illustrated in Figure 4. At the 1-ms pulse, channel 0 is sampled. After 5 µs, channel 2 is sampled. Channel 3 is sampled 5 µs after channel 2 is sampled. No samples are then taken until the next 1-ms pulse, when channel 0 is sampled again. In this mode, the rate for all channels is 1 kHz, but the channel-to-channel skew (delay) is now 5 µs, or 20 µs total. The minimum burst mode skew/delay on the PCI-DAS1602/16 is 5 µs.

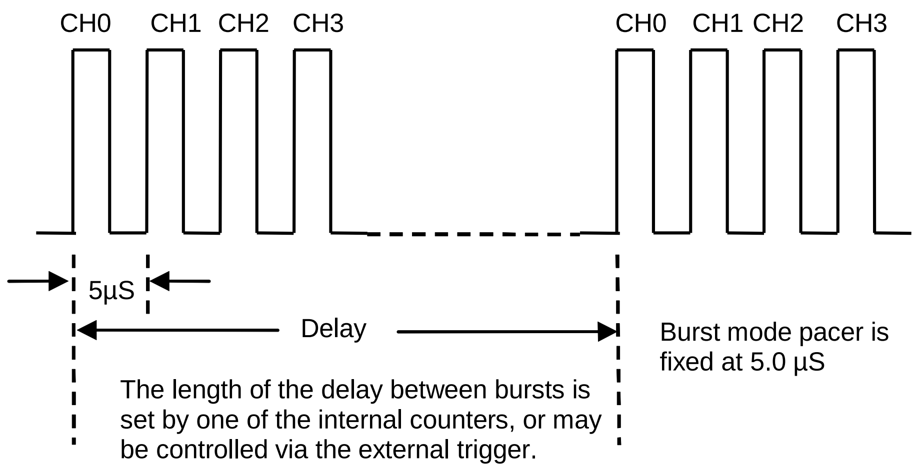

Figure 4. Burst mode timing

Analog outputs

The two high-speed 16-bit dual analog outputs are updated via an on-board FIFO and REP OUTSW commands, and provide a 100 kHz maximum update rate. Output ranges are individually configurable with software for ±10 V and ±5 V, 0 to 10 V and 0 to 5 V. The D/A outputs provide rated accuracy to ±5 mA, and are short circuit protected (25 mA limit). The analog outputs are cleared to 0 V on power up or reset.

Parallel digital I/O

The 24 bits of TTL-compatible, high-current (64 mA sink, 15 mA source) digital I/O are available as two eight-bit ports and two four-bit ports. This digital capability is an 82C55 mode 0 chip emulation, which allows each port to be configured independently as either input or output. The digital I/O ports default to the input state (high impedance) on power up or reset.

Counter/timer I/O

The PCI-DAS1602/16 provides two counter 82C54 counter chips. Each chip contains three 16-bit down counters that provide clock, gate, and output connections. You can connect the counter clock to the on-board 10 MHz crystal oscillator, or leave unconnected for user input.

Calibrating the PCI-DAS1602/16

The PCI-DAS1602/16 is equipped with software auto calibration. The *Insta*Cal software makes gain and offset corrections to the board using on-board digital potentiometers and trim D/A converters. No user intervention or external equipment is required. The PCI-DAS1602/16 is shipped fully-calibrated from the factory.

All adjustments are made via 8-bit calibration DACs or 7-bit digital potentiometers that are referenced to an on-board factory calibrated standard. Calibration factors are stored on the serial nvRAM. At run time, these calibration factors can be loaded into system memory and can be automatically retrieved when a different DAC/ADC range is specified

You can recalibrate with respect to the factory-measured voltage standards at any time by selecting the **Calibrate** menu in *Insta*Cal. Full calibration requires less than two minutes and requires no external equipment or user adjustments.

The standard calibration involves calibrating one channel with 0 volts input (offset), and then with a known input voltage (gain). The PCI-DAS1602/16's on board circuitry first shorts the inputs for offset calibration, then connects the inputs to the ultra-stable precision voltage reference for the gain calibration.

Analog input calibration

Analog inputs are calibrated for offset and gain. Offset calibration is performed directly on the input amplifier with trim DACs acting on the amplifier. Input gain calibration is performed with the precision voltage reference.

Front-end offset corrections are typically performed at the gain stage and/or the ADC input. Offset calibration is performed in the instrumentation amplifier gain stage. Front-end gain adjustment is only performed via the ADC reference, since the gain tolerance of the in-amp circuit is quite good, and there is adequate gain tuning range using only the ADC.

The analog input calibration system is shown in Figure 5.

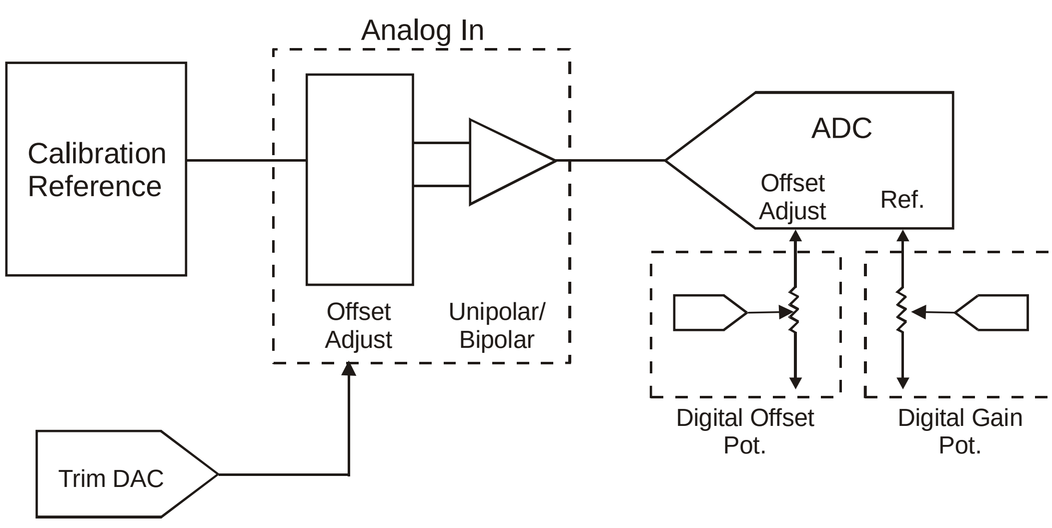

Figure 5. Analog input calibration

Analog output calibration

The analog output circuits are calibrated for both gain and offset. Offset adjustments for the analog outputs are made in the output buffer section. The tuning range of this adjustment allows for maximum DAC and output buffer offsets. Gain calibration of the analog outputs is performed via DAC reference adjustments.

The analog output calibration system is shown in Figure 6. This circuit is duplicated for both DAC0 and DAC1.

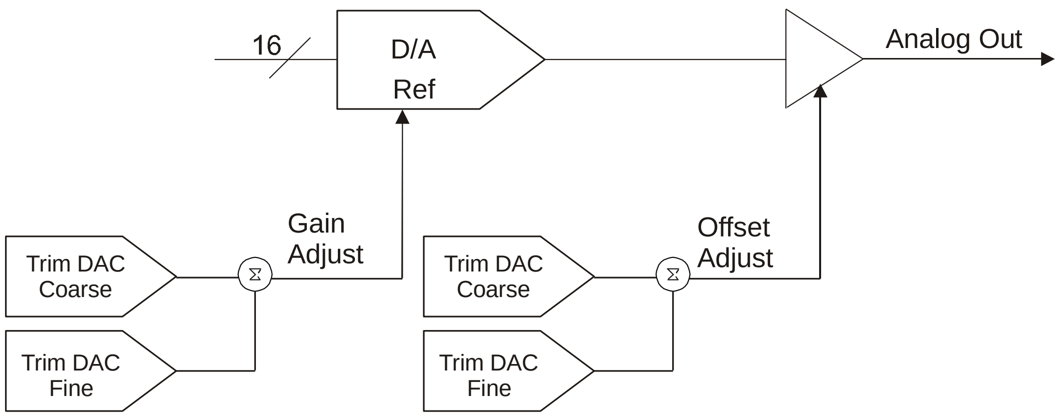

Figure 6. Analog output calibration

Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

All specifications are subject to change without notice.

Analog input

Table 1. Analog input specifications

A/D converter type	AD976ABN
Resolution	16 bits
Number of channels	16 single-ended / 8 differential, software selectable
Input ranges, software selectable	±10 V, ±5 V, ±2.5 V, ±1.25 V 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V
Polarity	Unipolar/bipolar, software selectable
A/D pacing (software programmable)	Internal counter - 82C54.
	External source (A/D EXTERNAL PACER)
	Software polled
Burst mode	Software selectable option, rate = 5 µs
A/D trigger sources	External digital (A/D EXTERNAL TRIGGER)
	External analog (ANALOG TRIGGER IN)
A/D triggering modes	External digital: Software configurable for: ▪ Edge (triggered) ▪ Level-activated (gated) ▪ Programmable polarity (rising/falling edge trigger, high/low gate)
	External analog: software-configurable for: ▪ Positive or negative slope. ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window Trigger levels set by DAC0 and/or DAC1, 4.88 mV resolution.
	Unlimited pre- and post-trigger samples. Total # of samples must be > 256. Compatible with both Digital and Analog trigger options.
Data transfer	From 512 sample FIFO via interrupt w/ REPINSW
	Interrupt
	Software polled
A/D conversion time	*5 µs max*
Throughput	200 kHz
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Common mode range	±10 V min
CMRR @ 60 Hz	-70 dB
Input leakage current	*±200 nA max*
Input impedance	*10 MΩ min*
Absolute maximum input voltage	*±15 V*

Accuracy

Table 2. Analog input accuracy specifications

Range	Accuracy
BIP10	±16 LSB
BIP5	±6 LSB
BIP2.5	±16 LSB
BIP1.25	±16 LSB
UNI10	±8 LSB
UNI5	±28 LSB
UNI2.5	±28 LSB
UNI1.25	±28 LSB
Accuracy Components	
Gain error	Trimmable by potentiometer to 0
Offset error	Trimmable by potentiometer to 0
PGA linearity error	*±1.3 LSB typ , ±10.0 LSB max*
Integral linearity error	±0.5 LSB typ , ±3.0 LSB max
Differential linearity error	±0.5 LSB typ, ±2.0 LSB max

Total board error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical absolute accuracy of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors is at their maximum level, and causing error in the same direction.

Analog input drift

Table 3. Analog input drift specifications

Range	Analog input full-scale gain drift	Analog input zero drift	Overall analog input drift
± 10.00 V	2.2 LSB/°C max	1.8 LSB/°C max	4.0 LSB/°C max
± 5.000 V	2.2 LSB/°C max	1.9 LSB/°C max	4.1 LSB/°C max
± 2.500 V	2.2 LSB/°C max	2.0 LSB/°C max	4.2 LSB/°C max
± 1.250 V	2.2 LSB/°C max	2.3 LSB/°C max	4.5 LSB/°C max
0 - 10.00 V	4.1 LSB/°C max	1.9 LSB/°C max	6.0 LSB/°C max
0 - 5.000 V	4.1 LSB/°C max	2.1 LSB/°C max	6.2 LSB/°C max
0 - 2.500 V	4.1 LSB/°C max	2.4 LSB/°C max	6.5 LSB/°C max
0 - 1.250 V	4.1 LSB/°C max	3.0 LSB/°C max	7.1 LSB/°C max

Absolute error change per °C temperature change is a combination of the Gain and Offset drift of many components. The theoretical worst case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors is at their maximum level, and causing error in the same direction.

Noise performance

The following table summarizes the worst case noise performance for the PCI-DAS1602/16. Noise distribution is determined by gathering 50000 samples with inputs tied to ground at the PCI-DAS1602/16 main connector. Data is for both single-ended and differential modes of operation.

Table 4. Noise specifications

Range	±2 counts	±1 count	Max Counts	LSBrms*
± 10.00 V	97%	80%	11	1.7
± 5.000 V	97%	80%	11	1.7
± 2.500 V	96%	79%	11	1.7
± 1.250 V	96%	79%	11	1.7
0 - 10.00 V	88%	65%	15	2.3
0 - 5.000 V	88%	65%	15	2.3
0 - 2.500 V	83%	61%	15	2.3
0 - 1.250 V	83%	61%	16	2.4

* Input noise is assumed to be Gaussian. An RMS noise value from a Gaussian distribution is calculated by dividing the peak-to-peak bin spread by 6.6.

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the specified per channel rate for a total of 50000 samples. A full scale 100 Hz triangle wave is input on channel 1. Channel 0 is tied to analog ground at the 100-pin user connector. Table 5 summarizes the influence of channel 1 on channel 0 and does not include the effects of noise.

Table 5. Crosstalk specifications

Range	1 kHz Crosstalk (LSB pk-pk)	10 kHz Crosstalk (LSB pk-pk)	50 kHz Crosstalk (LSB pk-pk)
±10.000 V	4	13	24
±5.000 V	2	7	18
±2.500 V	2	5	16
±1.250 V	3	4	14
0V to +10.000 V	4	8	23
0V to +5.000 V	2	5	16
0V to +2.500 V	2	4	16
0V to +1.250 V	3	3	16

Analog output

Table 6. Analog output specifications

D/A converter type	AD669BR
Resolution	16 bits
Number of channels	2
Channel type	Single-ended voltage output
Output range (each channel independently software selectable)	±10 V, ±5 V, 0 to 10 V, or 0 to 5 V
Data transfer	From 512 sample FIFO via REPOUTSW or programmed I/O. Data interleaved for dual analog output mode.
Throughput	100 kHz, 2 channels simultaneous
Monotonicity	*16 bits at 25 °C*
Slew rate	10 V ranges: 6 V/µs
	5 V ranges: 3 V/µs
Settling time	13 µS max 20 V step to 0.0008%
	6 µS typ 10V step to 0.0008%
Current drive	±5 mA min
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 ohms max
Output stability	Any passive load
Coding	Offset binary
Output voltage on power up and reset	0 V ± 10 mV

Accuracy

Table 7. Analog output accuracy specifications

Range	**Accuracy**
BIP10	±8 LSB
BIP5	±8 LSB
UNI10	±10 LSB
UNI5	±10 LSB
Accuracy Components	
Integral linearity error	±0.5 LSB typ, ±1 LSB max
Differential linearity error	*±0.5 LSB typ, ±1 LSB max*

Analog output drift

Table 8. Analog output drift specifications

Analog output full-scale gain drift	±0.22 LSB/°C max
Analog output zero drift	±0.22 LSB/°C max
Overall analog output drift	±0.44 LSB/°C max

Absolute error change per °C temperature change is a combination of the gain and offset drift of many components. The theoretical worst case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors is at their maximum level, and causing error in the same direction.

Digital input / output

Table 9. Digital input/output specifications

Digital type	82C55 emulation
	Input 74LS244
	Output 74LS373
Number of I/O	24
Configuration	2 banks of 8 and 2 banks of 4, or
	3 banks of 8, or
	2 banks of 8 with handshake
Input high	*2.0 volts min, 7 volts absolute max*
Input low	*0.8 volts max, -0.5 volts absolute min*
Output high	*2.4 volts min @ -15 mA*
Output low	*0.5 volts max @ 64 mA*
Power-up / reset state	Input mode (high impedance)
Pull-up/pull-down resistors	Provisions have been made on the board for user installed pull-up/pull-down resistor networks
Simultaneous sample and hold trigger	TTL output (SSH OUT). Logic 0 = Hold Logic 1 = Sample compatible with CIO-SSH16

Interrupts

Table 10. Interrupt specifications

Interrupt	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9052
Interrupt polarity	Active high level or active low level, programmable through PLX9052
Interrupt sources (software programmable)	External (rising TTL edge event)
	Residual counter
	A/D End-of-conversion
	A/D End-of-channel-scan
	A/D FIFO-not-empty
	A/D FIFO-half-full
	D/A FIFO-not-empty
	D/A FIFO-half-full

Counter

*Note: Pins 21, 24, and 25 are pulled to logic high via 10K resistors.

Table 11. Counter specifications

Counter type	82C54	
Configuration	Two 82C54 chips containing three 16-bit down counters each	
82C54A:		
Counter 0 — ADC residual sample counter.	Source:	ADC Clock.
	Gate:	Programmable source.
	Output:	End-of-Acquisition interrupt.
Counter 1 — ADC pacer lower divider	Source:	10 MHz oscillator
	Gate:	Tied to Counter 2 gate, programmable source.
	Output:	Chained to Counter 2 Clock.
Counter 2 — ADC pacer upper divider	Source:	Counter 1 Output.
	Gate:	Tied to Counter 1 gate, programmable source.
	Output:	ADC Pacer clock (if software selected), available at user connector.
82C54B:		
Counter 0 — pretrigger mode	Source:	ADC Clock.
	Gate:	External trigger
	Output:	End-of-Acquisition interrupt.
Counter 0 — non-pretrigger mode: user counter 4	Source:	User input at 100pin connector or internal 10MHz (software selectable)
	Gate:	User input at 100pin connector.
	Output:	Available at 100pin connector.
Counter 1 — DAC pacer lower divider	Source:	10 MHz oscillator
	Gate:	Tied to Counter 2 gate, programmable source.
	Output:	Chained to Counter 2 Clock.
Counter 2 — DAC pacer upper divider	Source:	Counter 1 Output.
	Gate:	Tied to Counter 1 gate, programmable source.
	Output:	DAC Pacer clock, available at user connector.
Clock input frequency	*10 MHz max*	
High pulse width (clock input)	*30 ns min*	
Low pulse width (clock input)	*50 ns min*	
Gate width high	*50 ns min*	
Gate width low	*50 ns min*	
Input high	*2.0 volts min, 5.5 volts absolute max*	
Input low	*0.8 volts max, -0.5 volts absolute min*	
Output high	*3.0 volts min @ -2.5 mA*	
Output low	*0.4 volts max @ 2.5 mA*	
Crystal oscillator frequency	10 MHz	
Frequency accuracy	50 ppm	

Power consumption

Table 12. Power consumption specifications

+5 V operating (A/D converting to FIFO)	2 A typical, 2.1 A max

Environmental

Table 13. Environmental specifications

Operating temperature range	0 to 70 °C
Storage temperature range	-40 to 100 °C
Humidity	0 to 95% non-condensing

Mechanical

Table 14. Mechanical specifications

Card dimensions	PCI custom type card: 107 mm (H) x 18.5 mm (W) x 292 mm (L)

Main connector and pin out

Table 15. Main connector specifications

Connector type	100-pin high-density, Robinson-Nugent
Compatible cables	C100FF-x
Compatible accessory products (with C100FF-x cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50 SSR-RACK24 (DADP-5037 adaptor required) SSR-RACK08 (DADP-5037 adaptor required) CIO-ERB24 (DADP-5037 adaptor required) CIO-ERB08 (DADP-5037 adaptor required)

Table 16. 8-channel differential mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 HI	52	FIRSTPORTA Bit 1
3	CH0 LO	53	FIRSTPORTA Bit 2
4	CH1 HI	54	FIRSTPORTA Bit 3
5	CH1 LO	55	FIRSTPORTA Bit 4
6	CH2 HI	56	FIRSTPORTA Bit 5
7	CH2 LO	57	FIRSTPORTA Bit 6
8	CH3 HI	58	FIRSTPORTA Bit 7
9	CH3 LO	59	FIRSTPORTB Bit 0
10	CH4 HI	60	FIRSTPORTB Bit 1
11	CH4 LO	61	FIRSTPORTB Bit 2
12	CH5 HI	62	FIRSTPORTB Bit 3
13	CH5 LO	63	FIRSTPORTB Bit 4
14	CH6 HI	64	FIRSTPORTB Bit 5
15	CH6 LO	65	FIRSTPORTB Bit 6
16	CH7 HI	66	FIRSTPORTB Bit 7
17	CH7 LO	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	N/C
31	N/C	81	N/C
32	N/C	82	N/C
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	N/C
36	D/A OUT 0	86	N/C
37	D/A GND 1	87	N/C
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	ANALOG TRIGGER IN	93	N/C
44	D/A EXTERNAL PACER IN	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	D/A INTERNAL PACER OUTPUT
47	N/C	97	EXTERNAL D/A PACER GATE
48	PC +5V	98	N/C
49	SSH OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

Table 17. 16-channel single-ended mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 HI	52	FIRSTPORTA Bit 1
3	CH8 HI	53	FIRSTPORTA Bit 2
4	CH1 HI	54	FIRSTPORTA Bit 3
5	CH9 HI	55	FIRSTPORTA Bit 4
6	CH2 HI	56	FIRSTPORTA Bit 5
7	CH10 HI	57	FIRSTPORTA Bit 6
8	CH3 HI	58	FIRSTPORTA Bit 7
9	CH11 HI	59	FIRSTPORTB Bit 0
10	CH4 HI	60	FIRSTPORTB Bit 1
11	CH12 HI	61	FIRSTPORTB Bit 2
12	CH5 HI	62	FIRSTPORTB Bit 3
13	CH13 HI	63	FIRSTPORTB Bit 4
14	CH6 HI	64	FIRSTPORTB Bit 5
15	CH14 HI	65	FIRSTPORTB Bit 6
16	CH7 HI	66	FIRSTPORTB Bit 7
17	CH15 HI	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	N/C
31	N/C	81	N/C
32	N/C	82	N/C
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	N/C
36	D/A OUT 0	86	N/C
37	D/A GND 1	87	N/C
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	ANALOG TRIGGER IN	93	N/C
44	D/A EXTERNAL PACER IN	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	D/A INTERNAL PACER OUTPUT
47	N/C	97	EXTERNAL D/A PACER GATE
48	PC +5V	98	N/C
49	SSH OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
Suite 1008
Norton, MA 02766
USA

Category: Information technology equipment.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS1602/16

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: Electromagnetic Compatibility, EN 61326-1:2006 (IEC 61326-1:2005)

Emissions: Group 1, Class B

- EN55022 (1995)/CISPR 22: Radiated and Conducted emissions.

Immunity: EN61326-1:2006, (IEC 61326-1:2005)

- EN61000-4-2 (2001): Electrostatic Discharge immunity.
- EN61000-4-3 (2002): Radiated Electromagnetic Field immunity.
- EN61000-4-4 (2004): Electric Fast Transient Burst immunity.
- EN61000-4-5 (2001): Surge immunity.
- EN61000-4-6 (2003): Radio Frequency Common Mode immunity.
- EN61000-4-11 (2004): Voltage Dip and Interrupt immunity.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in September, 2001. Test records are outlined in Chomerics Test Report #EMI3053.01. Further testing was conducted by Chomerics Test Services, Woburn, MA. 01801, USA in December, 2008. Test records are outlined in Chomerics Test report #EMI5241.08.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja

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